2.7V to 16V Hot Swap Controller with Current Sense Output

Preliminary Technical Data

ADM1171

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supply Voltages from 2.7 V to 16.5V**
- **Adjustable Analog Current Limit with Circuit Breaker**
- **Current Sense Output**
- **Fast Response Limits Peak Fault Current**
- **Automatic Retry or Latch-Off On Current Fault**
- **Adjustable Supply Voltage Power-Up Rate**
- **Charge Pumped Gate Drive for External N-FET Switch**
- **True Soft Start control of Initial Current Profile**
- **TIMER pin allows control over timing functions**
- **Undervoltage Lockout**
- **Adjustable Overvoltage Protection**
- **8-pin TSOT Package**

APPLICATIONS

- **Hot Swap Board Insertion – Line Cards, Raid systems**
- **Electronic Circuit Breaker**
- **Industrial High Side Switch/Circuit Breaker**

GENERAL DESCRIPTION

The ADM1171 is a Hot Swap controller that allows a board to be safely inserted and removed from a live backplane.

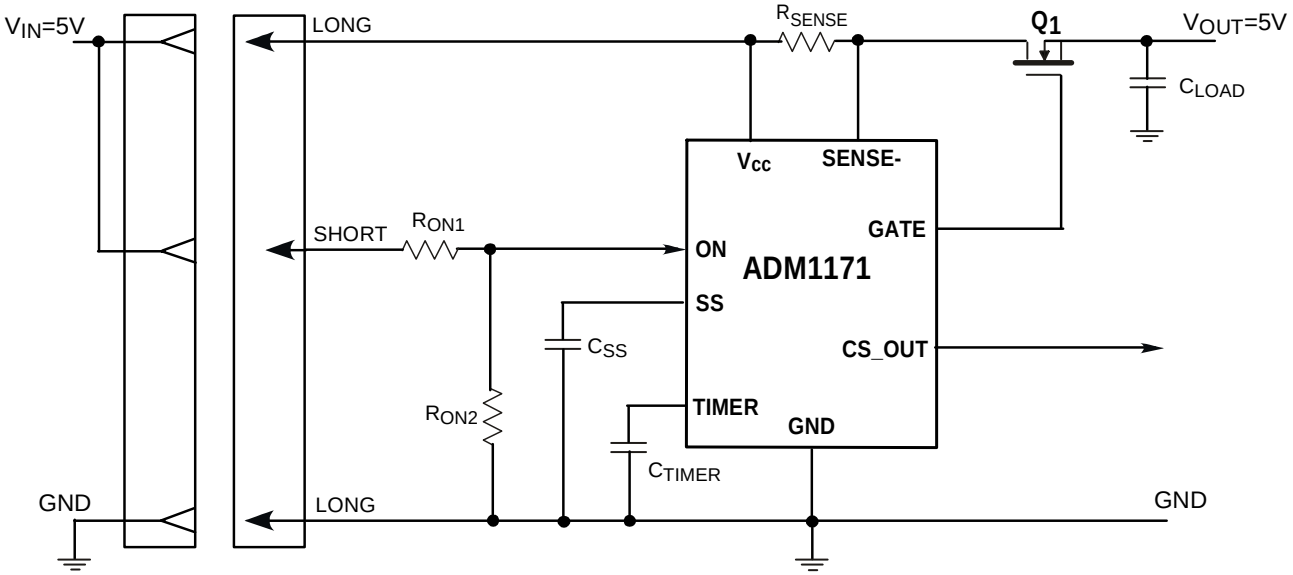
An internal charge pumped driver controls the GATE of an external high side N-channel FET for a supply voltage ranging from 2.7V to 16.5V. The ADM1171 provides the initial timing cycle and allows the GATE to be ramped up at an adjustable rate.

The ADM1171 features a fast current limit loop providing active current limiting together with a circuit breaker timer. The magnitude of the current can be determined by the voltage on the CSOUT pin. The signal at the ON pin turns the part on and off and is also used for the reset function.

The SS pin allows the user to control the soft start profile of the current ramp at start-up via an external capacitor.
A capacitor connected to the TIMER pin gives the user control over the duty cycle of the PWM retry ratio during current fault.

This part is available in two options: the ADM1171-1 will automatic retry for over-current fault and the ADM1171-2 will latch-off for an over-current fault.
The ADM1171 is packaged in an 8-lead TSOT package.

APPLICATIONS DIAGRAM



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ADM1171—SPECIFICATIONS

Table 1. V_{CC} = 2.7V to 16.5V, T_A = -40°C to +85°C, Typical Values at T_A = 25°C unless otherwise noted.

Parameter	Min	Typ	Max	Units	Conditions
V_{CC} Pin					
Operating Voltage Range, V_{CC}	2.7		16.5	V	
Supply Current, Icc		0.65	1.0	mA	
Undervoltage Lockout, V_{UVLO}	2.4	2.525	2.65	V	V_{CC} Rising
Undervoltage Lockout Hysteresis, $V_{UVLOHYS}$		25		mV	
ON Pin					
ON Pin Input Current, I_{INON}	-100	0	100	nA	
On Pin Threshold, V_{ON}	1.26	1.3	1.34	V	ON rising
ON Pin Threshold Hysteresis, V_{ONHYST}		80		mV	
RS- Pin					
SENSE Pin Input Current, $I_{INSENSE}$	10	20	30	µA	$V_{SENSE} = V_{CC}$
Circuit Breaker Limit Voltage, V_{CB}	44	50	56		$V_{CB} = (V_{CC} – V_{SENSE})$
Fast Current Limit Voltage	60	70			
RS- Pin					
Hot Swap Voltage	2.7		16.5	V	
RS- Pin Input Current, $I_{INSENSE}$	TBD	-200	TBD	µA	$V_{SENSE} = V_{CC}$, $V_{HOTSWAP}$ = 0.6 V, Note
	10	20	30	µA	$V_{SENSE} = V_{CC}$, $V_{HOTSWAP}$ > 2.2 V
Circuit Breaker Limit Voltage, V_{CB}	34	47	60	mV	$V_{CB} = (V_{CC} – V_{SENSE})$,$V_{HOTSWAP}$ = 0.6 V
	44	47	53	mV	$V_{CB} = (V_{CC} – V_{SENSE})$,$V_{HOTSWAP}$ > 2.2 V
Over Current Limit Voltage, V_{OC}	40	53	66	mV	$V_{HOTSWAP}$ = 0.6 V, Note
	50	53	59	mV	$V_{HOTSWAP}$ > 2.2 V
GATE Pin					
GATE Drive Voltage, V_{GATE}	5	6.5	10	V	$V_{GATE} – V_{CC}$, V_{CC} = 2.7V
GATE Drive Voltage, V_{GATE}	6	8	12	V	$V_{GATE} – V_{CC}$, V_{CC} = 5V
GATE Drive Voltage, V_{GATE}	5	6.5	10	V	$V_{GATE} – V_{CC}$, V_{CC} = 16.5V
Gate Pullup Current	10	12	14	uA	V_{GATE} = 0V
Gate Pulldown Current		2		mA	V_{GATE} = 3V, Vcc > UVLO
Gate Pulldown Current		25		mA	V_{GATE} = 3V, Vcc < UVLO
Soft Start (SS) Pin					
Soft Start Pullup Current		10		µA	
Current Setting Gain		20		V/V	Vss/Vsense
Soft Start Completion Voltage		1		V	
Pull-Down Current		100		µA	Fault
TIMER Pin					
TIMER Pin Pull-Up Current, $I_{TIMERUP}$	-4	-5	-6	µA	Initial Cycle, V_{TIMER} = 1V
	-48	-60	-72	µA	During Current Fault, V_{TIMER} = 1V
TIMER Pin Pull-Down Current, $I_{TIMERDN}$		2	2.5	µA	After Current Fault, V_{TIMER} = 1V
		100		µA	Normal Operation, V_{TIMER} = 1V
TIMER Pin Threshold High, V_{TIMERH}	1.235	1.3	1.365	V	TIMER rising
TIMER Pin Threshold Low, V_{TIMERL}	0.18	0.2	0.22	V	TIMER falling
CSOUT Pin					
Total Output Voltage Error	-5	0	5	%	VCC-SENSE = 100mV
Gain	19	20	21	V/V	VCC-SENSE = 10 to100mV
Output Impedance		25		KΩ	
Settling Time		1		µs	

Absolute Maximum Ratings

Table 2. ADM1171 Absolute Maximum Ratings

Parameter	**Rating**
V_{CC} Pin	20V
RS- Pins	-0.3V to 20V
TIMER Pin	-0.3V to (V_{CC} + 0.3V)
SS Pin	TBD
ON Pin	-0.3V to 20V
CSOUT	-0.3V to (V_{CC} + 0.3V)
GATE Pin	V_{CC} + 11V
Power Dissipation	TBD
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

HOT CIRCUIT INSERTION

When circuit boards are inserted into live backplanes, the supply bypass capacitors can draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, glitches on the system supply or reset other boards in the system.

The ADM1171 is designed to turn a printed circuit board's supply voltage ON and OFF in a controlled manner, allowing the circuit board to be safely inserted into or removed from a live backplane. The ADM1171 can reside either on the backplane or on the daughter board for hot circuit insertion applications.

OVERVIEW

The ADM1171 is designed to operate over a range of supplies from 2.7V to 16.5V. Upon insertion, an undervoltage lockout circuit determines if sufficient supply voltage is present. When the ON pin goes high an initial timing cycle assures that the board is fully seated in the backplane before the FET is turned on. A single timer capacitor sets the periods for all of the timer functions. After the initial timing cycle the ADM1171 can either start up in current limit or with a lower load current. Once the external FET is fully enhanced and the supply has ramped up, the ADM1171 monitors the load current through an external sense resistor. Overcurrent faults are actively limited to 47mV/R_{SENSE} for a specified circuit breaker timer limit. The ADM1171-1 will automatically retry after a current limit fault while the ADM1171-2 latches off. The ADM1171-1 timer function limits the retry duty cycle to 3.8% for FET cooling.

UNDERVOLTAGE LOCKOUT

An internal undervoltage lockout (UVLO) circuit resets the ADM1171 if the V_{CC} supply is too low for normal operation. The UVLO has a low-to-high threshold of 2.525V, a 25mV hysteresis. Above 2.525V supply voltage, the ADM1171 will start if the ON pin conditions are met.

ON FUNCTION

The ON pin is the input to a comparator which has a low-to-high threshold of 1.3V, an 80mV hysteresis and a high-to-low glitch filter of 30μs and a low-to-high glitch filter of 3us. A low input on the ON pin resets the ADM1171 TIMER status and turns off the external FET by pulling the GATE pin to ground. A low-to-high transition on the ON pin starts an initial cycle followed by a start-up cycle. A 10k pull-up resistor connecting the ON pin to the supply is recommended. The 10k resistor shunts any potential static charge on the backplane and reduces the overvoltage stress at the ON pin during live insertion.

Alternatively, an external resistor divider at the ON pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit. An RC filter can be added at the ON pin to increase the delay time at card insertion if the internal glitch filter delay is insufficient.

GATE FUNCTION

During hot insertion of the PCB, an abrupt application of supply voltage charges the external FET drain/gate capacitance. This can cause an unwanted gate voltage spike. An internal circuit holds GATE low before the internal circuitry wakes up. This reduces the FET current surges substantially at insertion. The GATE pin is held low in reset mode and during the initial

timing cycle. In the start-up cycle the GATE pin is pulled up by a 12μA current source. During an over-current fault condition, the error amplifier servos the GATE pin to maintain a constant current to the load until the circuit breaker trips. When the circuit breaker trips, the GATE pin shuts down abruptly.

CURRENT LIMIT CIRCUIT BREAKER FUNCTION

The ADM1171 features a current limiting circuit breaker. When there is a sudden load current surge, such as a low impedance fault, the bus supply voltage can drop significantly to a point where the power to an adjacent card is affected, causing system malfunctions. The ADM1171 high bandwidth current control loop limits current by reducing the external FET GATE pin voltage. This minimizes the bus supply voltage drop and permits power budgeting and fault isolation without affecting neighbouring cards.

CALCULATING CURRENT LIMIT

The nominal fault current limit is determined by a sense resistor connected between V_{CC} and the SENSE pin as given by the equation below:

$$I_{LIMIT(NOM)} = V_{CB(NOM)} / R_{SENSE} \quad (1)$$

The minimum load current is given by Equation 2:

$$I_{LIMIT(MIN)} = V_{CB(MIN)} / R_{SENSE(MAX)} \quad (2)$$

The maximum load current is given by Equation 3:

$$I_{LIMIT(MAX)} = V_{CB(MAX)} / R_{SENSE(MIN)} \quad (3)$$

Note: The power rating of the sense resistor should be rated at the fault current level.

For proper operation, the minimum current limit must exceed the circuit maximum operating load current with margin. The sense resistor power rating must exceed $V_{CB(MAX)}^2 / R_{SENSE(MIN)}$.

TIMER FUNCTION

The TIMER pin handles several key functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: COMP1 (0.2V) and COMP2 (1.3V). The four timing current sources are:

- 5μA pull-up
- 60μA pull-up
- 2μA pull-down
- 100μA pull-down

The 100μA is a non-ideal current source approximating a 7k resistor below 0.4V.

INITIAL TIMING CYCLE

When the card is being inserted into the bus connector, the long pins mate first which brings up the supply VIN at time point 1 of Figure 3. The ADM1171 is in reset mode as the ON pin is low. GATE is pulled low and the TIMER pin is pulled low with a 100μA source. At time point 2, the short pin makes contact and ON is pulled high. At this instant, a start-up check requires that the supply voltage be above UVLO, the ON pin beabove1.3Vand the TIMER pin voltage be less than 0.2V. When these three conditions are fulfilled, the initial cycle begins and the TIMER pin is pulled high with 5μA. At time point 3, the TIMER reaches the COMP2 threshold and the first portion of the initial cycle ends. The 100μA current source then pulls down the TIMER pin until it reaches 0.2V at time point 4. The initial cycle delay (time point 2 to time point 4) is related to C_{TIMER} by equation:

$$t_{INITIAL} \sim= 272.9 \times C_{TIMER} \text{ ms/uF} \quad (4)$$

When the initial cycle terminates, a start-up cycle is activated and the GATE pin ramps high. The TIMER pin continues to be pulled down towards ground.

CURRENT SENSE OUT

The ADM1171 has a Current Sense Output. The voltage across the VCC/RS- pins is amplified by a factor of 20 and is output on this pin. This can then be fed to an ADC and the magnitude of the current flowing through the sense resistor can be obtained.

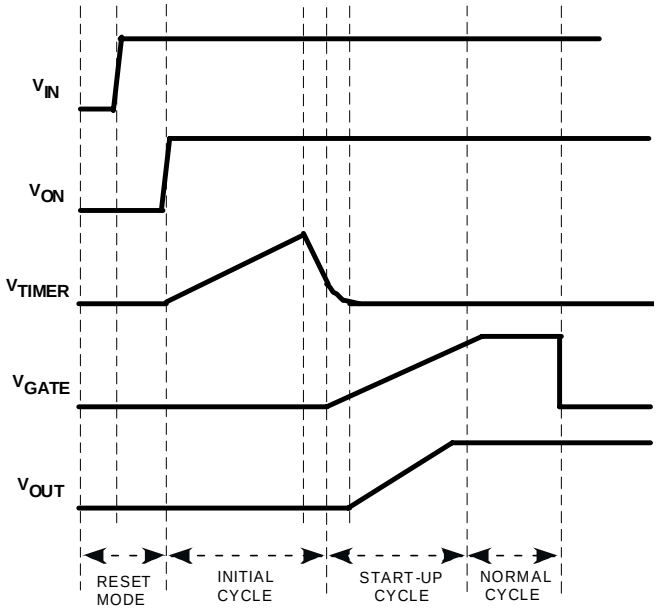


Figure 1: Normal Start-up

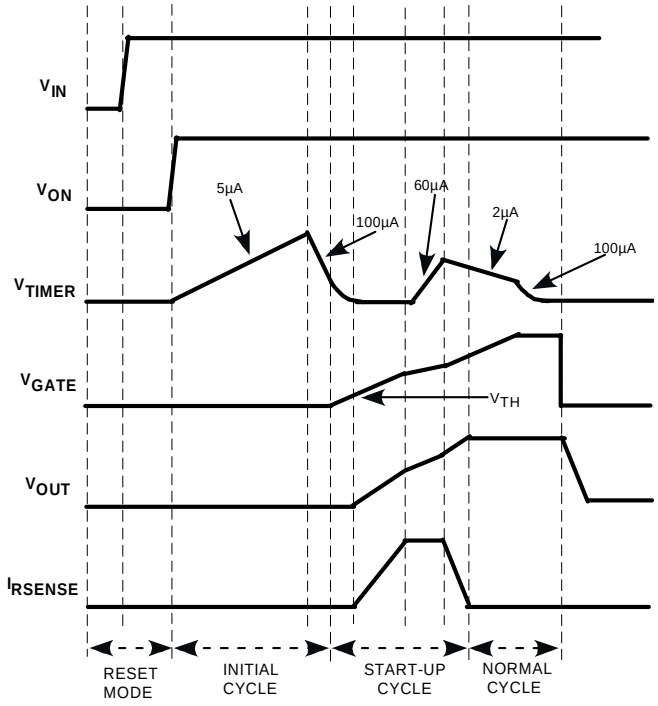


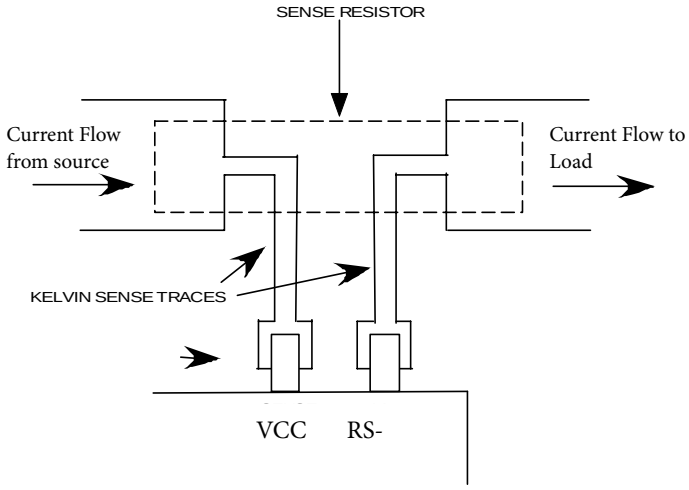
Figure 2: Current Limiting at Start-up

SOFT START (SS PIN)

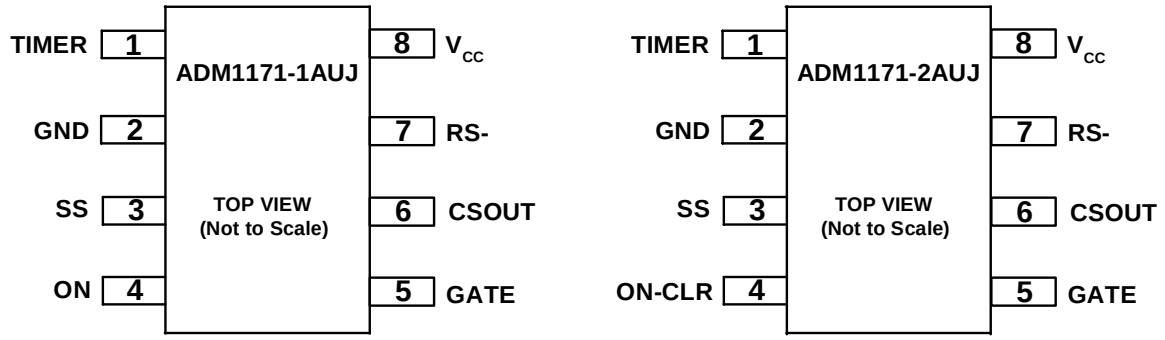
The SS pin is used to determine the inrush current profile. A capacitor should be attached to this pin. Whenever the FET is requested to turn on, the SS pin is held at ground until the SENSE pin reaches a few mV. A current source is then turned on, which linearly ramps the capacitor up to 1V. The reference voltage for the GATE linear control amplifier is derived from the soft start voltage, such that the inrush linear current limit is defined as: : $I_{LIMIT} = V_{SS} / (20 \times R_{SENSE})$

KELVIN SENSE RESISTOR CONNECTION

When using a low-value sense resistor for high current measurement the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 18 below shows the correct way to connect the sense resistor between the VCC and RS- pins of the ADM1171.



PIN CONFIGURATIONS



PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Name	Description
1	TIMER	Timer Input Pin. An external capacitor C_{TIMER} sets a 272.9ms/µF initial timing delay and a 21.7ms/µF circuit breaker delay. The GATE pin turns off whenever the TIMER pin is pulled beyond the upper threshold, such as for overvoltage detection with an external zener.
2	GND	Chip Ground Pin
3	SS	Soft Start pin. An external capacitor between the SS pin and GND sets the ramp rate of the load current profile at initial connection.
4	ON (ON-CLR)	Input Pin. The ON pin comparator has a low-to-high threshold of 1.3V with 80mV hysteresis and a glitch filter. When the ON pin is low, the ADM1171 is reset. When the ON pin goes high, the GATE turns on after the initial timing cycle. On the ADM1171-2, a rising edge on this pin has the added function of clearing a fault and restarting the device
5	GATE	GATE Output Pin. This pin is the high side gate drive of an external N-channel FET. An internal charge pump provides a 12µA pull-up current with Zener clamps to RS+ and ground. In overload, the error amplifier (EA) controls the external FET to maintain a constant load current.
6	CSOUT	Current Sense Analog voltage Output. This voltage represents the amplified differentail voltage across the VCC and RS- pins.
7	R S-	Current Limit Sense Input Pin. A sense resistor between the Vcc and RS- pins sets the analog current limit. In overload, the EA controls the external FET gate to maintain the SENSE voltage at 47mV. When the EA is maintaining current limit, the TIMER circuit breaker mode is activated. The current limit loop/circuit breaker mode can be disabled by connecting the Vcc pin and RS- pin together.
8	V_{CC}	Positive Supply Input Pin. The operating supply voltage range is between 2.7V to 16.5V. An undervoltage lockout (UVLO) circuit with a glitch filter resets the ADM1171 when a low supply voltage is detected.

OUTLINE DIMENSIONS

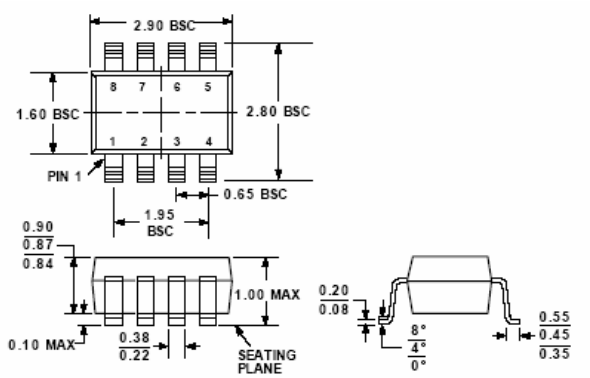


Figure 3. 8-Lead TSOT Package (UJ-8)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 3. Ordering Guide

Part Number	Version	Temperature Package	Package Description	Package Outline
ADM1171-1AUJ	Automatic Retry Version	–40°C to +85°C	TSOT	UJ-8
ADM1171-2AUJ	Latched Off Version	–40°C to +85°C	TSOT	UJ-8

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